



**JUNE 23-27, 2024**

MOSCONE WEST CENTER  
SAN FRANCISCO, CA, USA



**SYNOPSYS®**  
Silicon to Software™



JUNE 23-27, 2024

MOSCONE WEST CENTER  
SAN FRANCISCO, CA, USA

# Beyond digital: innovation in symbolic simulator to empower IO analog circuit validation

Pawan Verma<sup>1</sup>, Manish Bansal<sup>1</sup>, Anil Kumar Dwivedi<sup>1</sup>  
Amandeep Kaur<sup>2</sup> Hari Sathianathan<sup>2</sup>

<sup>1</sup>STMicroelectronics

<sup>2</sup>Synopsys Inc.



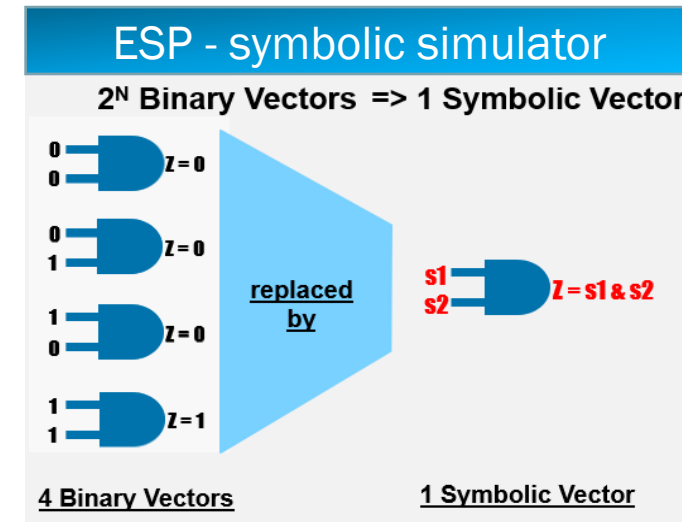
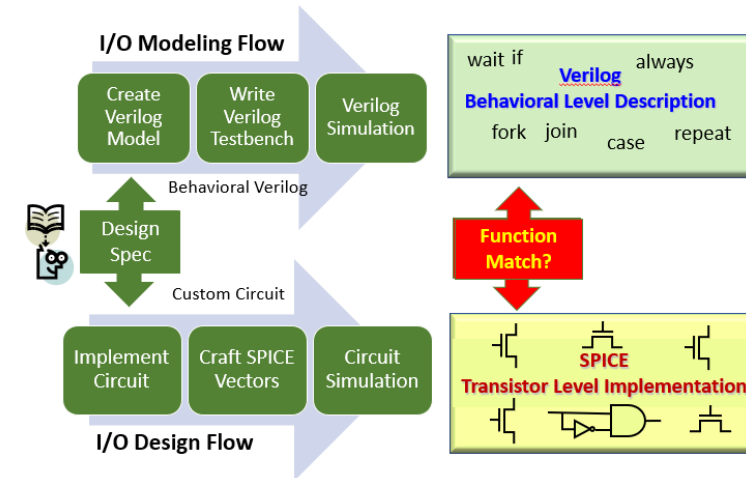
# Motivation & challenges

## Motivation

- IO designs becoming more complex–mix of analog & digital architectures used
  - Lead behavioral model is not directly schematic-driven but to be written manually
- Validation of schematic & behavior models are done individually
  - Emerges need to validate their functional alignment

## Synopsys ESP Solution challenges with IO designs

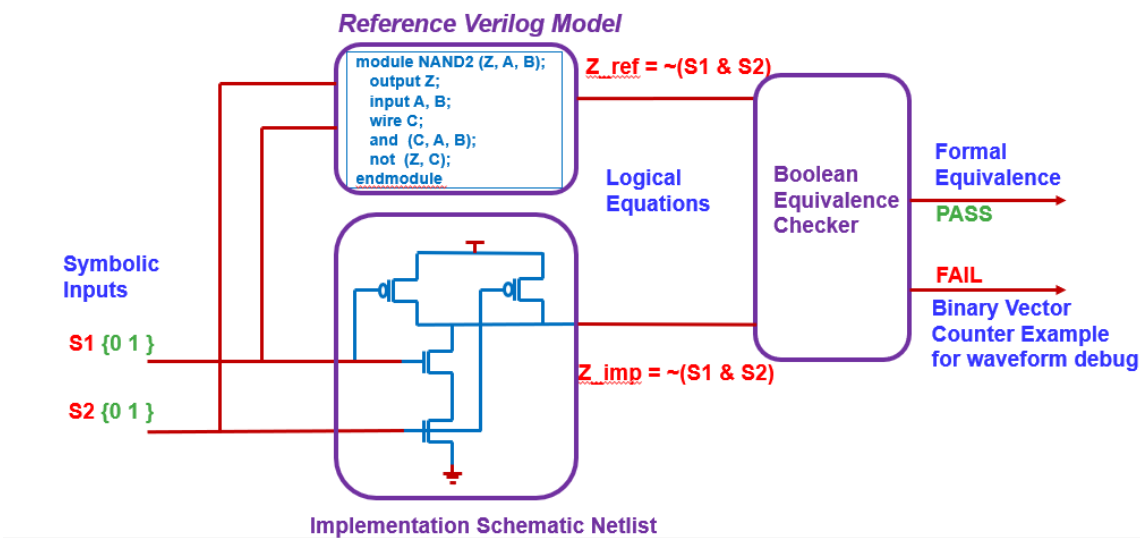
- ESP works on creating boolean-equation and performing symbolic simulation
  - Managing digital blocks with boolean-equation is straightforward for ESP
  - Evaluating IO designs having analog circuits can be more difficult to accomplish
- Without resolving analog blocks accurately, ESP leading into false errors



The goal is to address design architecture having more analog behavior, to improve ESP validation coverage

# ESP: advantages over traditional flow

## Symbolic simulation flow



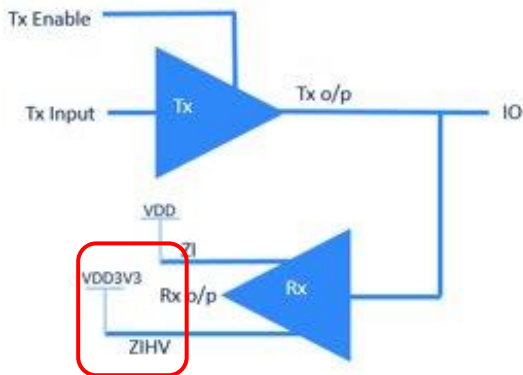
- Formal equivalence checking based on symbolic simulation
- Boolean expressions compared with output of MODEL & SPICE
- Coverage report is dumped that shows % coverage & verification gaps
- Identify unconventional corner cases, not caught by traditional flow

## Real modeling errors caught by ESP

### Rx-pin functionality mismatch

Supply-pins		Input	Output
VDD	VDD3V3	IO	ZIHV
0	1	?	L

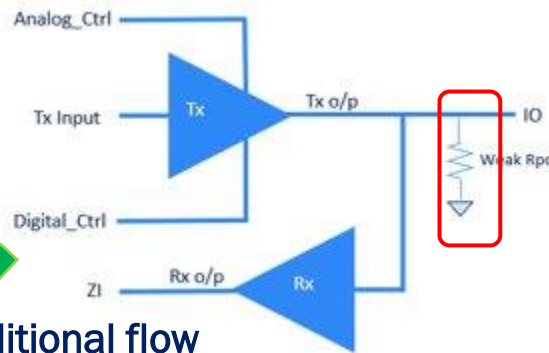
Supply-cond		Input	Output
VDD	VDD3V3	IO	ZIHV
0	1	0	0
		1	1



### Missing weak pull-down modeling

Input		Output (IO)	
Analog_Ctrl	Digital_Ctrl	Verilog	Schematic
0	0	Z	L(Weak pull-Down)

Input		Output (IO)	
Analog_Ctrl	Digital_Ctrl	Verilog	Schematic
0	0	L(Weak pull-Down)	L(Weak pull-Down)



These errors were not caught by the traditional flow

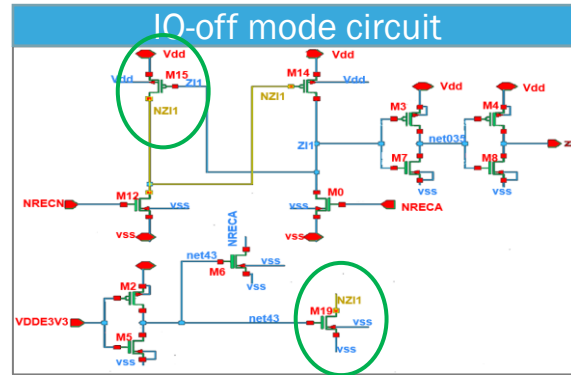
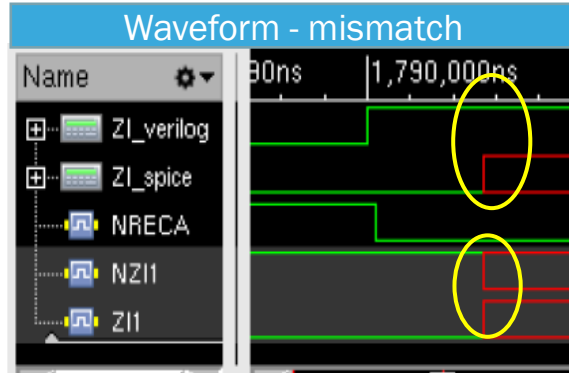
Symbolic simulation delivers high coverage functional verification

# Challenges in validating IO design with analog behavior (1/2)

## Challenge 1: design with power-down mode

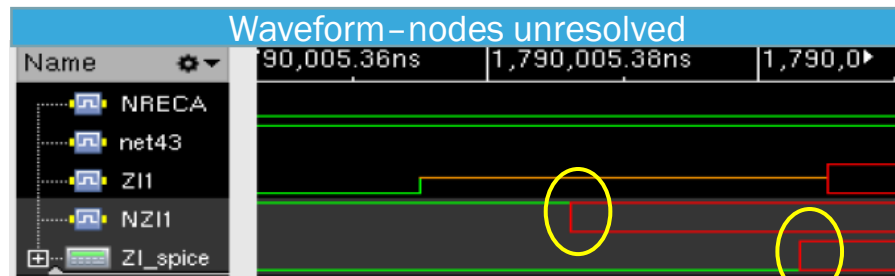
O/p pin ZI modeled as “1” in Verilog, ESP reported “x” in spice

- Internal node NZI1 resolved to logic “x” by ESP(expected 0)



The state of NZI1 is decided by the states of M15(PMOS) & M19(NMOS)

- PMOS turned off & NMOS took longer time to pull down, resulted into NZI1=x by ESP



Due to the strength difference of NMOS & PMOS, ESP reported a false error

## Solution: pattern matching feature

The strength of NMOS should be rectified to drive the NZI1 correctly.

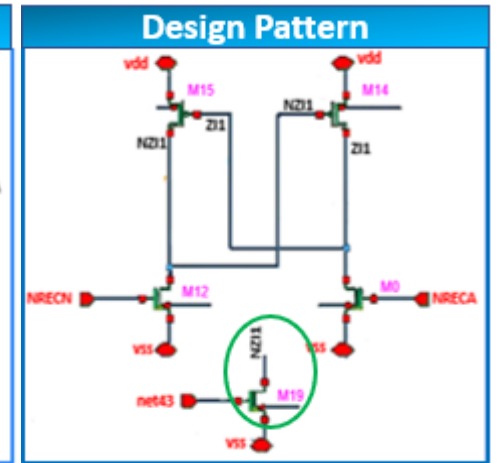
ESP supports a pattern matching technique—to identify design pattern

- Include a specific circuit-pattern with commands in the flow.

**Sample pattern Match File**

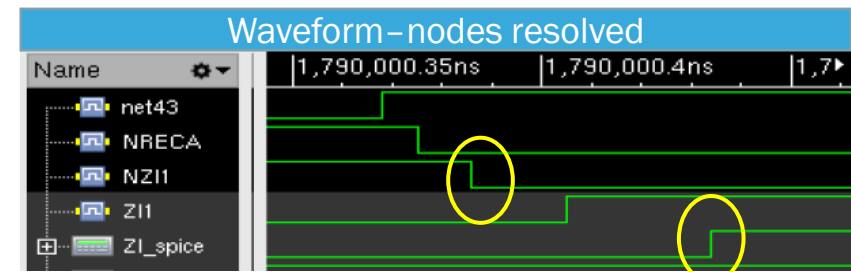
```
**innoprop pmmatch parameter off;
** innoprop inst rcscalestr 5 b2b MM19;

.subckt b2b ZI1 NZI1 NRECN net43 NRECA
MM14 ZI1 NZI1 vdd vdd psvtlp
MM15 NZI1 ZI1 vdd vdd psvtlp
MM12 NZI1 NRECN vss vss nsvt25
MM0 ZI1 NRECA vss vss nsvt25
MM19 NZI1 net43 vss vss nsvt25
.ends b2b
```



Commands are executed when the pattern is encountered

- NMOS(M19) strength 5x → net NZI1 evaluates to “0” instantly
- Logic “0” at NZI1 drives ZI1 to “1” → ZI=1

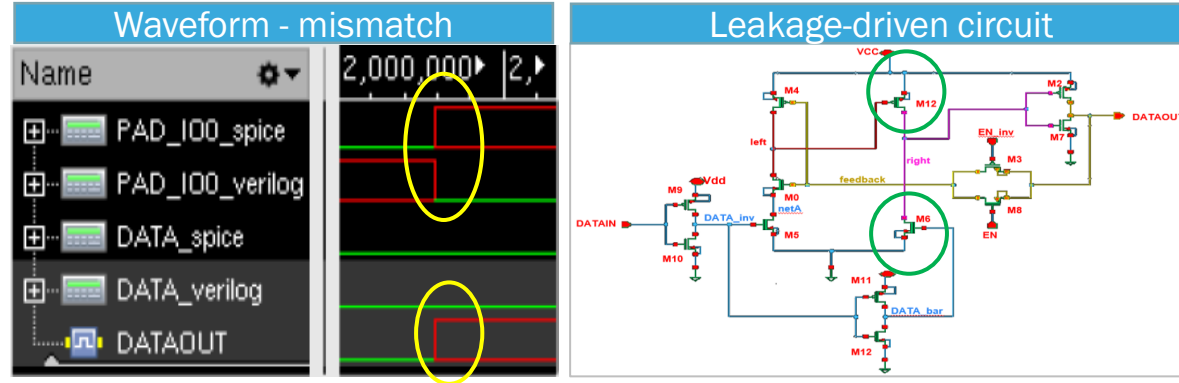


# Challenges in validating IO design with analog behavior (2/2)

## Challenge 2: design with leakage-driven node

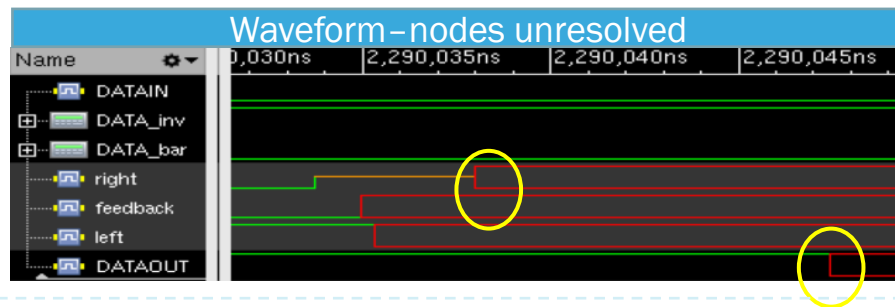
O/p pin PAD\_I00 modeled as “0” in Verilog, ESP reported “x” in spice

- Internal node DATAOUT resolved to logic “x” by ESP(expected 0)



DATAOUT is driven by “right” node–connected to off-state devices

- right node, expected to be “0” through leakage-current (strong NMOS)–settled to “x” by ESP (*undriven(z) for some-time*).



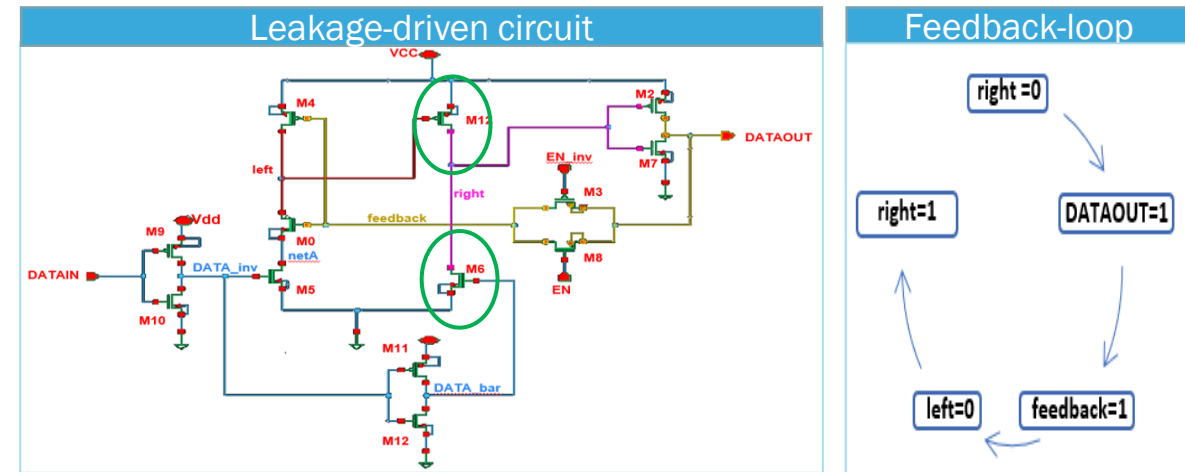
Due to wrong interpretation “x” of the leakage node, ESP reported a false error

## Solution: overriding x node to intended logic

Leakage-driven node “right” should be driven to “0” instead of x

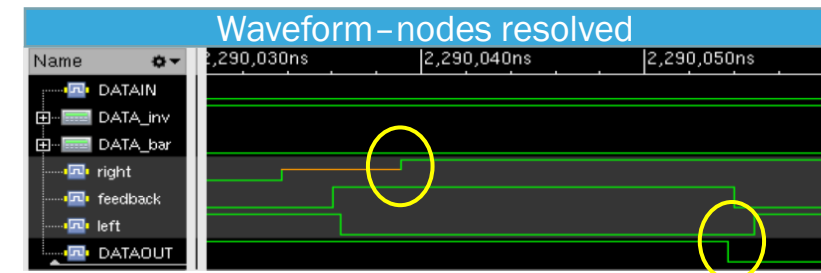
Identify “right” in design & treat as logic “0” using the command

`set_net_x-i-as 0 -design <subckt-name> right`



Command identifies *right* in design and initialize with logic 0

- right=0 → feedback loop → resolved to right=1
- Logic “1” at right drives DATAOUT to “0” → PAD\_I00=0



# Summary & results

Key points	Details
Pattern matching feature	Automated topology evaluations → enhance accuracy & mitigate false errors (Introduced architectures are generic and used across > 50% of the IO portfolio)
Command mastery	Commands like <b>set_net_x</b> for resolution of leakage-driven nodes <b>broaden ESP validation</b> coverage
Validation success rate	Collaborative efforts resulted in successfully validating 80% of IO analog designs
Parallel processing	Library-level (~10-15 cells) validation runtime reduced to ~30min (2 to 3 days) through distributed processing

## Work in progress

- To support devices with more than four terminals
- Intermediate voltage level handling for differential blocks



JUNE 23-27, 2024

MOSCONE WEST CENTER  
SAN FRANCISCO, CA, USA

# Thank you!

